

REMARKS

Claims 1, 9-17, 21, and 22 are presently active.

In the Office Action dated 27 May 2003 ("Office Action"), claims 9 and 10 were rejected under 35 U.S.C. §102(b) as being anticipated by Hariton, US patent 5,926,064 ("Hariton"); claim 9 was rejected under 35 U.S.C. §103(a) as obvious over Bazzani, US patent 6,087,896 in view of Millman, "Microelectronics: Digital and Analog Circuits and Systems," 1979, McGraw-Hill, page 237; claims 11 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hariton; claims 13-16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art Fig. 2 in view of Hariton; and claims 1, 17, 21, and 22 were allowed.

Applicant acknowledges with appreciation the allowance of claims 1, 17, 21, and 22.

Before specifically addressing the claim rejections, Applicant would like to respectfully point out the distinction between the terms "coupled" and "connected". To someone of ordinary skill in the art of circuit design, these two terms have different scopes. To a circuit designer, the ordinary meaning of "A is connected to B" is that A and B are connected by a passive structure for making a direct electrical connection so that the voltage potential of A and B are substantially equal to each other. For example, A and B may be connected by way of an interconnect, transmission line, etc. In integrated circuit technology, the "interconnect" may be exceedingly short, comparable to the device dimension itself. For example, the gates of two transistors may be connected to each other by polysilicon or copper interconnect that is comparable to the gate length of the transistors.

To a circuit designer, the ordinary meaning of "A is coupled to B" is that either A and B are connected to each other as described above, or that, although A and B may not be connected to each other, there is nevertheless a device or circuit that is connected to both A and B. This device or circuit may include active or passive circuit elements. For example, part of a circuit may include the description that the gate of transistor A is connected to the cathode of a diode, and that the anode of the diode is connected to the gate of transistor B. According to such a description, one may broadly recite that the gate

of transistor A is coupled to the gate of transistor B. However, such a recitation does not, by itself, mean that A is connected to B.

Clearly, the term "coupled" is broader in scope than the term "connected".

Applicant respectfully asks the question: If "connected" were to be interpreted as broadly as "coupled", then how could one ever precisely describe a circuit by reciting merely its structure? Clearly, it is possible to precisely and unambiguously describe a circuit by merely reciting its structure. This preciseness is accomplished by using the term of art "connected".

Furthermore, Applicant respectfully points out that use of the transition term "comprising" in claim drafting does not alter the meaning of the term of art "connected". The use of "comprising" merely means that other elements, not claimed, may fall within the scope of the claim. For example, the recitation "A is connected to B" in open-ended claiming does not preclude the possibility that the scope of the claim may cover another element that is also connected or coupled to A and/or B.

Turning now to the claim rejections, Hariton neither teaches nor suggests the claimed invention. Referring to Fig. 5 of Hariton, the gate of nMOSFET 505 is connected to the gate of nMOSFET 506 and the drain of nMOSFET 505. The drain of nMOSFET 505 is connected to the drain of pMOSFET 504. However, the gate and drain of nMOSFET 505 are not connected to the sources and drains of transistors 302 and 303.

Accordingly, Applicant does not believe that Hariton is applicable to the claimed invention.

To better define the invention, claims 9, 11, 13, and 15 are amended to recite that the gates of the first and second field effect transistors are not connected to each other. In Bazzani, the gates of the first and second FETs are connected to each other. As a result, Applicant believes that the claims are clearly distinguishable over Bazzani.

Respectfully submitted,

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